REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1 – 33 are currently pending in the present application. By way of this reply, claims 1, 12, and 23 have been amended.

II. Claim Amendments

Independent claim 1 has been amended to clarify that (i) the estimating is dependent on the inputting, and (ii) the adjusting is dependent on the estimating. No new matter has been added by way of these amendments.

Independent claim 12 has been amended to clarify that the computer system is caused, at least in part, to (i) estimate jitter of the delay locked loop dependent on the representative power supply waveform having noise, and (ii) adjust an amount of decoupling capacitance dependent on the estimate. No new matter has been added by way of these amendments.

Independent claim 23 has been amended to clarify that the instructions are adapted, at least in part, to (i) estimate jitter of the delay locked loop dependent on the representative power supply waveform having noise, and (ii) adjust an amount of decoupling capacitance dependent on the estimate. No new matter has been added by way of these amendments.

III. Double Patenting Rejection(s)

Claims 1 – 33 of the present application were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 33 of copending U.S. Patent Application No. 10/075,757. However, this rejection is improper because U.S. Patent Application No. 10/075,757 is not prior art to the present application. Both the present application and U.S. Patent Application No. 10/075,757 were filed on February 14, 2002. In order to sustain an obviousness-type double patenting rejection, each invalidating reference must be prior art. This is not the case here as U.S. Patent Application No. 10/075,757 is not prior art to the present application. Accordingly, this rejection is improper and withdrawal of same is respectfully requested.

IV. Rejection(s) Under 35 U.S.C § 103

Claims 1 – 6, 12 – 17, and 23 – 27

Claims 1 – 6, 12 – 17, and 23 – 27 of the present application were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,446,016 issued to Zhu (hereinafter "Zhu") in view of Applicant's Admitted Prior Art (hereinafter "AAPA"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a technique for optimizing decoupling capacitance in a delay locked loop. *See* Specification, paragraph [0020]. One or more embodiments of the present invention relate to the use of a representative power supply waveform having noise as an excitation into a simulation of a delay locked loop. *See*

Specification, paragraph [0021]. By using a representative power supply waveform having noise, an estimate of jitter is determined. *See id.* The estimate of jitter of the delay locked loop is used to adjust an amount of decoupling capacitance. *See id.* These steps may be iterated until the jitter falls below some level. *See id.*

Accordingly, amended independent claim 1 of the present application requires, in part, (i) estimating jitter of a delay locked loop *dependent* on an input representative power supply waveform having noise, and (ii) adjusting an amount of decoupling capacitance *dependent* on the estimating. Independent claims 12 and 23 have been amended with similar language, albeit in different form.

Zhu, in contrast to the present invention, fails to disclose at least the limitations of the claimed invention discussed above. Zhu discloses a technique for (i) adding a decoupling capacitor for a noisy node that violates a noise threshold, and (ii) incrementally increasing a size of the decoupling capacitor as the noise node continues to violate the threshold upon successive evaluations. *See, e.g.*, Zhu, Abstract. However, as specifically stated by the Examiner, Zhu fails to disclose inputting a power supply waveform having noise or estimating jitter of a delay locked loop as required by amended independent claims 1, 12, and 23 of the present application. *See* instant Office Action, page 5.

Like Zhu, AAPA fails to disclose each and every limitation of the claimed invention. Further, AAPA fails to supply that which Zhu lacks. In paragraph [0006] of the Specification (referenced by the Examiner on page 6 of the instant Office Action), the concept of "jitter" is described. Further, in paragraph [0024] of the Specification (referenced by the Examiner on page 5 of the instant Office Action), modeling power

supply noise is described. However, this combination of features in the Specification does not disclose as prior art *estimating* jitter *dependent* on an input power supply waveform having noise, and then adjusting a decoupling capacitance *dependent* on the estimating as required by amended independent claims 1, 12, and 23 of the present application. To the extent that Zhu may be argued as applying, Applicant notes that Zhu is directed to ensuring that margins for *noise*, not *jitter* (those skilled in the art will readily recognize that noise relates to amplitude imperfections and jitter relates to time imperfections), are met. Moreover, Zhu does not disclose *estimating* noise; instead, Zhu discloses adjusting decoupling capacitance based on whether noise on a node exceeds a particular threshold. This is entirely distinct from performing a step of *estimating*. Thus, neither AAPA nor Zhu disclose a step of estimating jitter dependent on an input power supply waveform having noise, and then adjusting decoupling capacitance dependent on the estimating as required by amended independent claims 1, 12, and 23 of the present application.

In view of the above, Zhu and AAPA, whether considered separately or in combination, fail to show or suggest the present invention as recited in amended independent claims 1, 12, and 23 of the present application. Thus, amended independent claims 1, 12, and 23 are patentable over Zhu and AAPA. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 7 – 11, 18 – 22, and 29 – 33

Claims 7 – 11, 18 – 22, and 29 – 33 of the present application were rejected under

35 U.S.C. § 103(a) as being unpatentable over Zhu in view of AAPA and U.S. Patent No. 6,370,678 issued to Culler (hereinafter "Culler"). For the reasons set forth below, this rejection is respectfully traversed.

As discussed above, Zhu and AAPA fail to disclose each and every limitation of amended independent claims 1, 12, and 23 of the present application. Like Zhu and AAPA, Culler fails to disclose each and every limitation of the claimed invention. Further, Culler fails to disclose that which Zhu and AAPA lack.

Culler discloses a technique for adjusting the logic synthesis process of IC design that takes into account the interaction between IC core logic circuitry, on-chip power supply circuitry, and package power supply circuitry. *See* Culler, Abstract. Culler is completely silent as to estimating jitter dependent on an input power supply waveform, and then adjusting decoupling capacitance dependent on the estimating as required by amended independent claims 1, 12, and 23 of the present application. Accordingly, Culler fails to disclose those limitations of the claimed invention not disclosed in Zhu and AAPA.

In view of the above, Zhu, AAPA, and Culler, whether considered separately or in any combination, fail to show or suggest the present invention as recited in amended independent claims 1, 12, and 23 of the present application. Thus, amended independent claims 1, 12, and 23 are patentable over Zhu, AAPA, and Culler. Dependent claims 7 – 11, 18 – 22, and 29 – 33 are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

V. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.163001; P7058).

Dated:

Respectfully submitted,

By _____

Wasif H. Qureshi
Registration No.: 51,048
OSHA • LIANG LLP
1221 McKinney St., Suite 2800
Houston, Texas 77010
Telephone: 408.730.2650
Attorney for Applicant

127386_1